

Precision low noise dual operational amplifier

Features

- Large output voltage swing
+14.3V/-14.6 V
- Low input offset voltage 850 μ V max.
- Low voltage noise: 4.5 nV/ $\sqrt{\text{Hz}}$
- High gain bandwidth product: 15 MHz
- High slew rate: 7 V/ μ s
- Low distortion: 0.002 %
- ESD internal protection 2 kV
- Excellent frequency stability
- Macromodel included in this specification



N
DIP8

(Plastic Package)



D
SO8

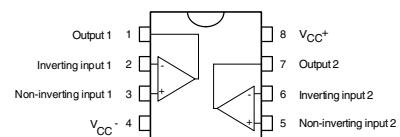
(Plastic Micropackage)

Description

The TS522 is a monolithic dual operational amplifier mainly dedicated to audio applications. The TS522 offers a very low input offset voltage as well as low voltage noise (4.5 nV/ $\sqrt{\text{Hz}}$) and high dynamic performances (15 MHz gain bandwidth product, 7 V/ μ s slew rate).

The output stage allows a large output voltage swing and symmetrical source and sink currents.

Pin connections top view



1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	±18 to 36	V
V_{id}	Differential input voltage ⁽¹⁾	±30	V
V_i	Input voltage ⁽¹⁾	±15	V
	Output short-circuit duration ⁽²⁾	Infinite	
T_j	Maximum junction temperature	+ 150	°C
T_{stg}	Storage temperature range	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient ^{(3) (4)} SO-8 DIP8	125 85	°C/W
R_{thjc}	Thermal resistance junction to case ^{(3) (4)} SO-8 DIP8	40 41	°C/W
ESD	HBM: human body model ⁽⁵⁾	2	kV
	MM: machine model ⁽⁶⁾	200	V
	CDM: charged device model ⁽⁷⁾	1.5	kV

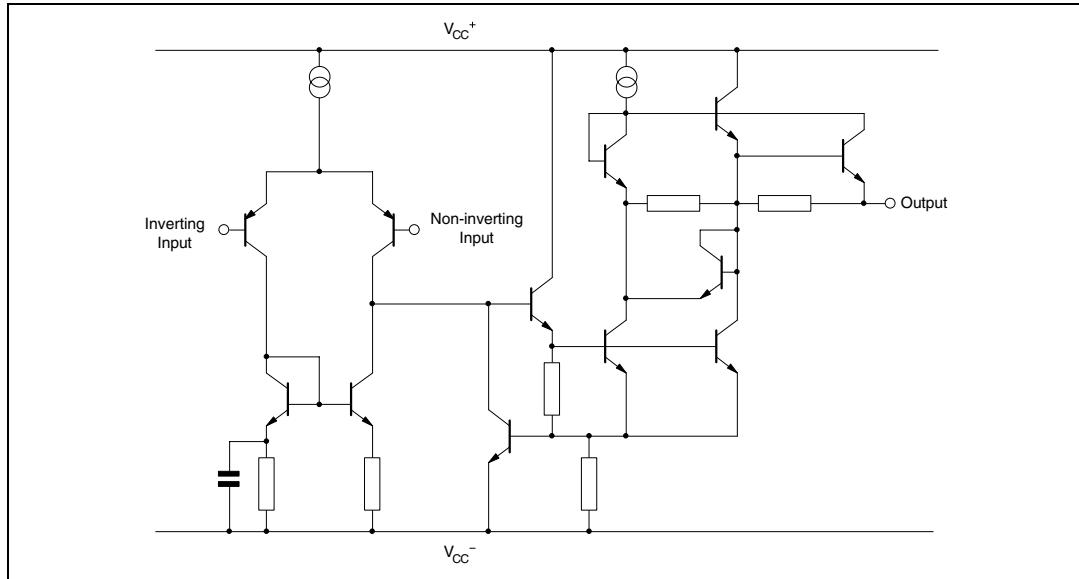
1. Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-
2. Power dissipation must be considered to ensure maximum junction temperature (T_j) is not exceeded.
3. Short-circuits can cause excessive heating and destructive dissipation.
4. R_{th} are typical values.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
7. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	±2.5 to ±15	V
T_{oper}	Operating free-air temperature range	-40 to 125	°C

2 Schematic diagram

Figure 1. Typical schematic diagram (1/2 TS522)



3 Electrical characteristics

**Table 3. $V_{CC+} = 15 \text{ V}$, $V_{CC-} = -15 \text{ V}$, $T_{amb} = 25^\circ \text{ C}$
(unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage ($V_o = 0\text{V}$, $V_{ic} = 0\text{V}$) $T_{amb} = +25^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$			0.85 1.7	mV
ΔV_{io}	Input offset voltage drift $V_{ic} = 0\text{V}$, $V_o = 0\text{V}$, $T_{min} \leq T_{amb} \leq T_{max}$		2		$\mu\text{V}/^\circ\text{C}$
I_{io}	Input offset current ($V_{ic} = 0\text{V}$, $V_o = 0\text{V}$) $T_{amb} = +25^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$		10	150 175	nA
I_{ib}	Input bias current ($V_{ic} = 0\text{V}$, $V_o = 0\text{V}$) $T_{amb} = +25^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$		250	750 800	nA
V_{icm}	Common mode input voltage range ($\Delta V_{io} = 5\text{mV}$, $V_o = 0\text{V}$)	± 13	± 14		V
A_{vd}	Large signal voltage gain ($R_L = 2\text{k}\Omega$, $V_o = \pm 10\text{V}$) $T_{amb} = +25^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$	90 85	100		dB
$\pm V_{opp}$	Output voltage swing ($V_{id} = \pm 1\text{V}$) $R_L = 600\Omega$ $R_L = 600\Omega$		12.2 -12.7		V
	$R_L = 2.0\text{k}\Omega$ $R_L = 2.0\text{k}\Omega$	13.2	14 -14.2	-13.2	
	$R_L = 10\text{k}\Omega$ $R_L = 10\text{k}\Omega$	13.5	14.3 -14.6	-14	
CMR	Common mode rejection ratio ($V_{ic} = \pm 13\text{V}$)	80	100		dB
SVR	Supply voltage rejection ratio $V_{CC+}/V_{CC-} = +15\text{V}/-15\text{V}$ to $+5\text{V}/-5\text{V}$	80	105		dB
I_o	Output short circuit current ($V_{id} = \pm 1\text{V}$, Output to ground) Source Sink	15 20	29 37		mA
I_{cc}	Supply current ($V_o = 0\text{V}$, all amplifiers) $T_{amb} = +25^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$		4	5 5.5	mA
SR	Slew rate ($V_i = -10\text{V}$ to $+10\text{V}$, $R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$, $A_V = +1$)	5	7		$\text{V}/\mu\text{s}$
GBP	Gain bandwidth product ($f = 100\text{kHz}$, $R_L = 2\text{k}\Omega$, $C_L = 100\text{pF}$)	10	15		MHz
B	Unity gain bandwidth (open loop)		9		MHz

**Table 3. $V_{CC+} = 15$ V, $V_{CC-} = -15$ V, $T_{amb} = 25^\circ$ C
(unless otherwise specified) (continued)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
A_m	Gain margin ($R_L = 2\text{k}\Omega$) $C_L = 0\text{pF}$ $C_L = 100\text{pF}$		-11 -6		dB
ϕ_m	Phase margin $C_L = 0\text{pF}$ $C_L = 100\text{pF}$		55 30		Degrees
e_n	Equivalent input noise voltage ($R_s = 100\Omega$, $f = 1\text{kHz}$)		4.5		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
i_n	Equivalent input noise current ($f = 1\text{kHz}$)		0.5		$\frac{\text{pA}}{\sqrt{\text{Hz}}}$
THD	Total harmonic distortion $R_L = 2\text{k}\Omega$, $f = 20\text{Hz}$ to 20kHz , $V_o = 3\text{V}_{\text{rms}}$, $A_V = +1$		0.002		%
V_{o1}/V_{o2}	Channel separation ($f = 20\text{Hz}$ to 20kHz)		120		dB
FPB	Full power bandwidth ($V_o = 27\text{V}_{\text{pp}}$, $R_L = 2\text{k}\Omega$, THD $\leq 1\%$)		120		kHz
Z_o	Output impedance ($V_o = 0\text{V}$, $f = 9\text{MHz}$)		37		Ω
R_i	Input resistance ($V_{ic} = 0\text{V}$)		175		$\text{k}\Omega$
C_i	Input capacitance ($V_{ic} = 0\text{V}$)		12		pF

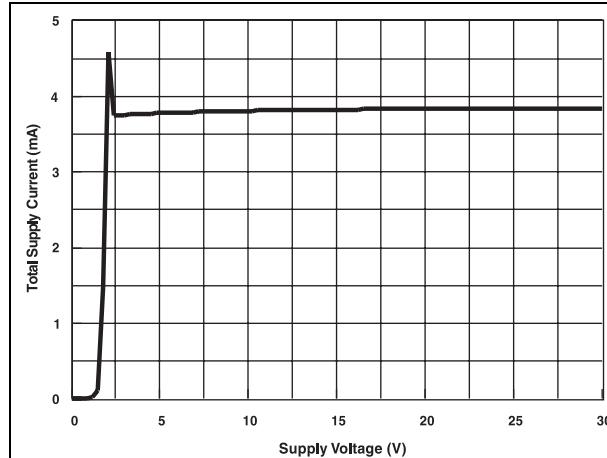
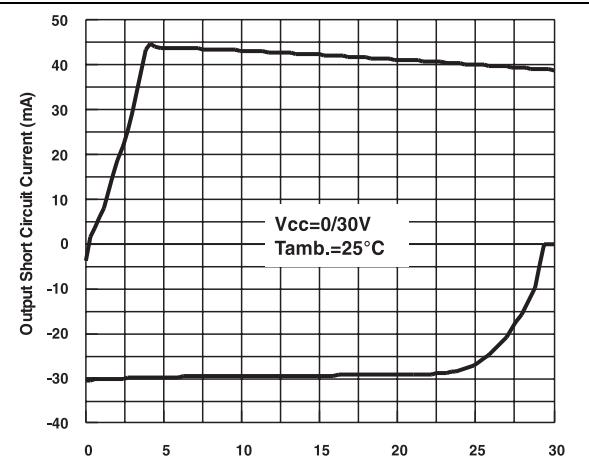
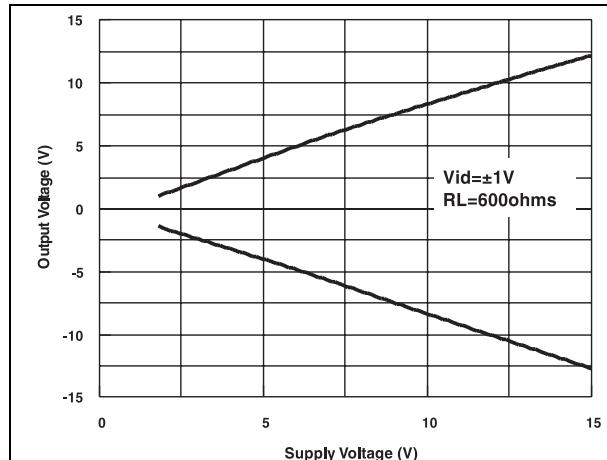
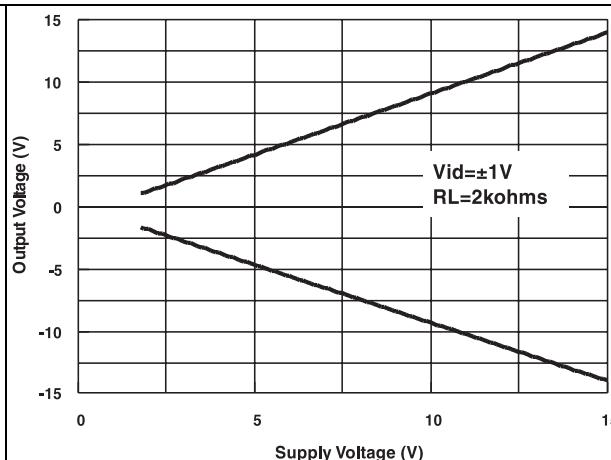
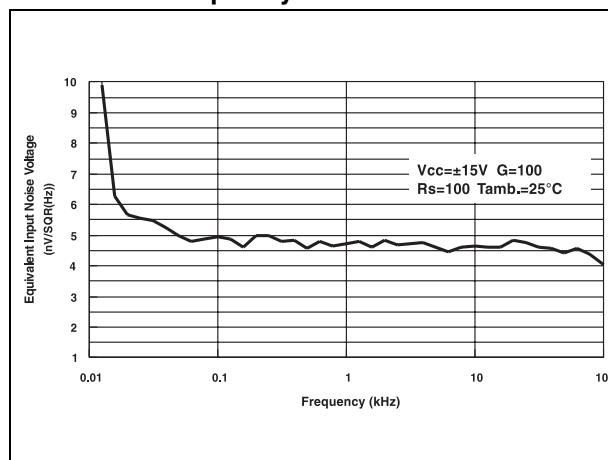
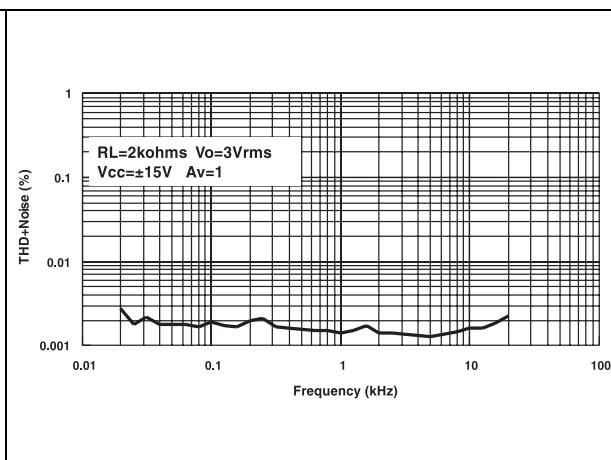
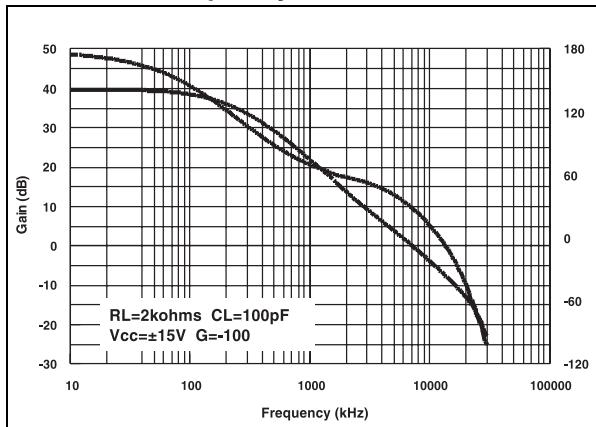
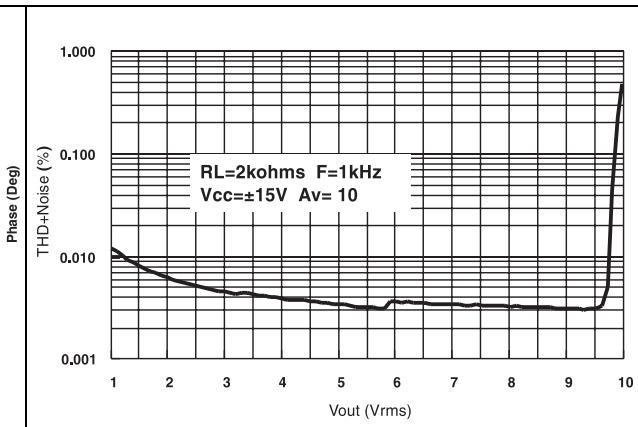
Figure 2. Total supply current vs supply voltage**Figure 3. Output short circuit current vs output voltage****Figure 4. Output voltage vs supply voltage****Figure 5. Output voltage vs supply voltage****Figure 6. Equivalent input noise voltage vs frequency****Figure 7. THD + Noise vs frequency**

Figure 8. Voltage gain and phase vs frequency**Figure 9. THD + Noise vs Vout**

4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 10. DIP8 package mechanical drawing

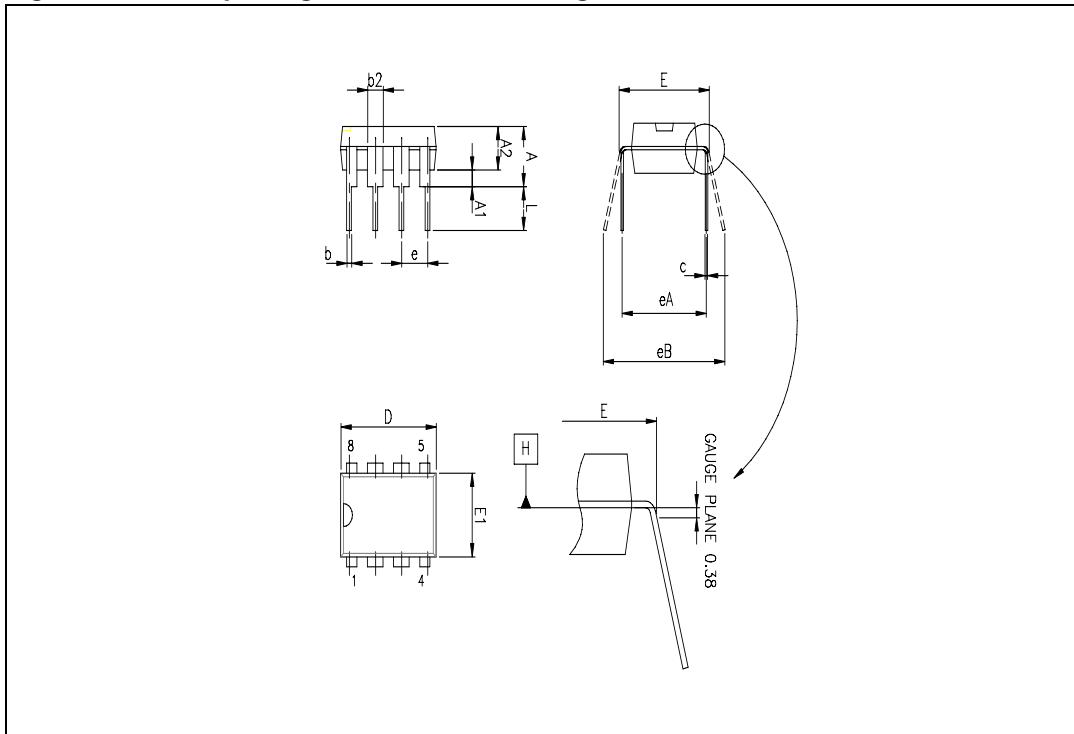


Table 4. DIP8 package mechanical data

Ref.	Dimensions			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

Figure 11. SO-8 package mechanical drawing

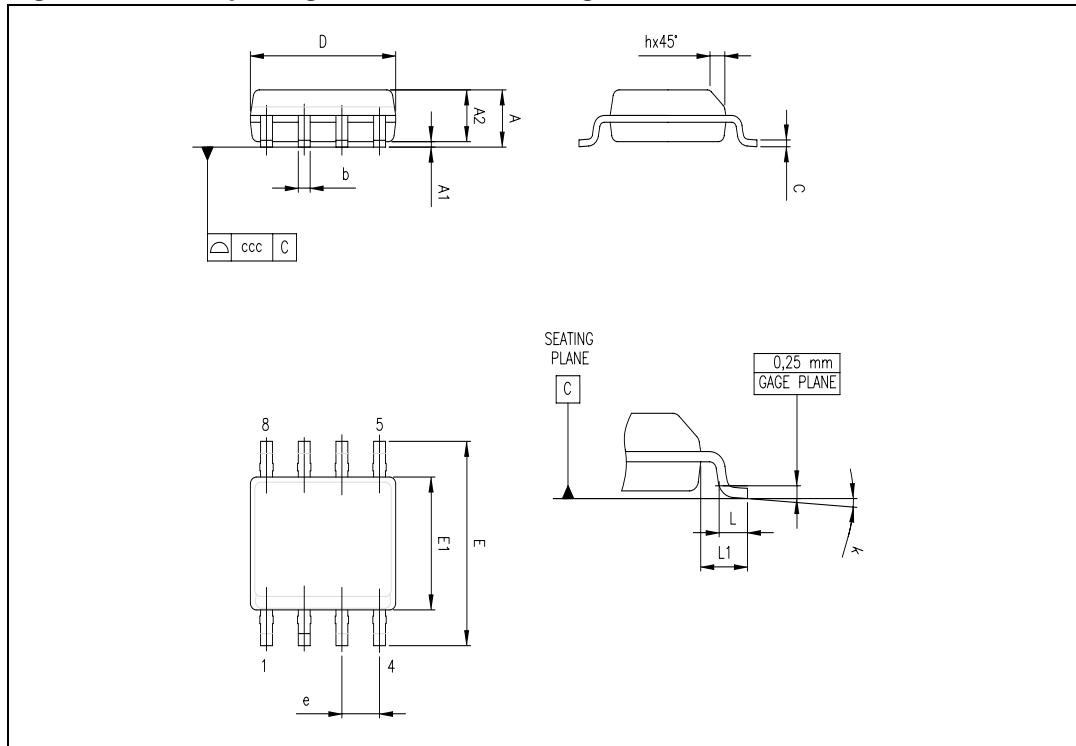


Table 5. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

5 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
TS522ID/DT	-40°C to +125°C	SO-8	Tube/tape & reel	522I
TS522IN	-40°C to +125°C	DIP8	Tube	TS522IN
TS522IYD/DT ⁽¹⁾	-40°C to +125°C	SO-8 (Automotive grade)	Tube/tape & reel	522IY

1. Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent.

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
01-Nov-2001	1	Initial release.
14-Oct-2008	2	Document reformatted. Added automotive grade order codes in Table 6: Order codes . Removed macromodel.

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